

SYSTOLICS ALGORITHMS: AN APPLICATION TO IMAGE SEGMENTATION

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ABSTRACT.

Developments in microelectronics and VLSI technology have result, at constrained cost, in multiprocessor architectures through which it is possible speed up algorithms in order to solve problems of high computational complexity.

In particular, systolic array architectures, have shown to be valuable for signal elaboration and digital imaging applications.

In this paper, after introducing the principal characteristics of systolic architectures, we present an applicative example of digital image segmentation.

different data.

We can fit on the SIMD class: systolic arrays and architectures composed by a grid of simple equal processors regularly connected among them.

The number of connections of a single processor with its neighbouring processors define the several spatial topologies of the array.

In fig. 1, we show several topologies obtained on 2-D space.

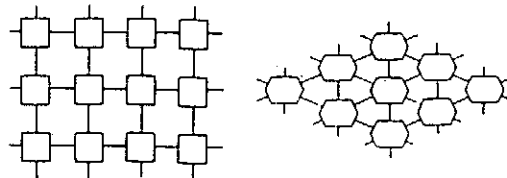


Fig. 1 Systolic arrays topologies on 2-D space

The term "systolic" has been named in accordance with its analogy with the systolic phases of the heart model. On every "cycle" of the system, each processor of the array receives data from the neighbouring processors, performs some local elaboration, and sends again the data to the linked processors, producing in this way a regular, continuous data flow through the whole array. There is no yet universal definition of systolic array, but we can characterize such an architecture by several properties always present:

- 1) Synchronization: all processors work in a synchronous among them.
- 2) Regularity: the processors are identical and identically linked among them.
- 3) Modularity: give us the possibility to extend in a random way the array adding moduli with other processors.
- 4) Linear speed-up: the elaboration speed increases li-

INTRODUCTION.

The different families of parallel architectures purposed up to now, can be fit into the two big categories: "single instruction multiple data" (SIMD) and "multiple instruction multiple data" (MIMD) so called multiprocessors. Typically an MIMD architecture is composed of several processors working in parallel on the given data and independently from each other. Naturally, the overhead associated to the physical interconnection puts a limit on the number of independent processors which can be linked to the system.

On the contrary, in SIMD architectures, different processors collaborate among them to reach a determined task, executing the same instruction simultaneously on

nearly with the number of processors configuring the arrays. Properties 1 and 2 give us a relative simplification of the VLSI circuit design implementing systolic arrays, while properties 3 and 4 ensure high performance levels and freedom from the physical dimension of the processors array.

Different prototypes of systolic architectures have been proposed by the electronics industry to allow researchers to apply and test them in real problem solving. Even if such implementation have had an experimental character (only recently systems with higher number of processors have been constructed) several classes of systolic array are now defined, and we can talk of many generation of them. A first differentiation can be done between single/multi-purpose and programmable systems.

In the first one there exists already a predefined and precodified number of designed elaborations "ad hoc" for a certain class of specific problems (e.g. matrix computation); in the limiting case where real time requirements exist, the design is cut off for the specific problem, as for example, DFT calculation.

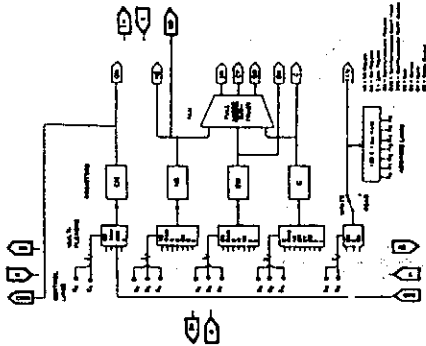
Systems belonging to the second class (programmable arrays) offer, obviously, a higher utilization flexibility, with many application, being possible to define, once a while, the execution program. In more evolved systems the same processor interconnection topology can be redefined via software before start of computation.

In the programmable array class reenters the development system GAPP (Geometric Arithmetic Parallel Processor) designed at the "Martin Marietta Aerospace Center" of Orlando (Fl.). Such a system as been adopted by the authors for the development and the testing of systolic algorithms for digital images elaboration. In the next paragraph we consider a synthetic designation of the HW/SW characteristics of the GAPP system.

GAPP DEVELOPMENT SYSTEM.

In this system have been assembled on a single board 144 processors organized on a 12x12 bidimensional array. Every processor has an own ALU configuration (full adder-subtractor), 4 operative registers, 128 bits of RAM, and 4 lines of communication which allows communication with its 4 linked processors (North, East, South, West). In fig.2 is illustrated the functional architecture of a single processor, while fig.3 shows the Active communication lines among the 4 adjacent processors. On the system, besides the control circuit and the interface towards the host computer, there is an I/O bus which permits to load or download data from processors without interfering the functioning of the ALU. This characteristics helps further to increase the performance

Fig.2 Internal architecture of a Processor element



of the system.

A processor employs approximately 2.6 μs to add two numbers represented on 8 bits; executing simultaneously 144 such operation, we obtain a global time of over 50M. additions for second. The real computational power and the acceleration of the throughput with the GAPP can be put in evidence during image elaboration being possible with such architecture to elaborate 144 pixels of the image in parallel.

Let us consider a simple algorithm as that of two images addition. Let A and B be two images of dimension NxN and let us construct the image C resulting of the addition of A and B, every pixel of C result to be defined by the relation:

$$C(i,j) := A(i,j) + B(i,j) \quad i, j = 1, 2, \dots, N$$

The execution of such an algorithm on a Von-Neuman sequential architecture requires exactly NxN machine cycles; the same algorithm executed on a GAPP architecture requires (NxN)/144 machine cycles. In an similar way is possible to verify that the Sobel transform calculation like other local transformation on a set of 144 pixels requires 800 cycles on the GAPP, against 12000 required by a typical sequential architecture execution.

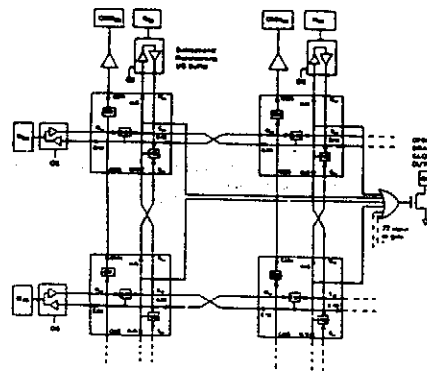


Fig. 3 Communication lines among 4 processor elements.

Several systolic algorithm, from the bottom to top levels, have been designed to exploit the GAPP computational speed. In the next paragraph we are going to describe an interesting application to the problem of image segmentation.

AN ALGORITHM FOR IMAGE SEGMENTATION.

The problem of digital image segmentation is a fundamental step for any automatic pattern recognition process.

The scope of the segmentation process can be substantially different according the image type to be analyzed and it is evidently linked to the analysis to be performed on the image.

For instance in the image elaboration of cytogenetic sample the segmentation must allow us to extract and identify several biological components (cells, read or white cells, chromosomes, etc.). In the other case like the robotic vision, the segmentation requires a deeper analysis and it is asked for the identification of the single components, areas or regions forming the pictorial scene to be analyzed.

Formally, the problem can be considered as labeling pro-

cess by which it is possible to assign to each pixel of the input image an identificative value (label) of the region to which the pixel belongs.

In the related literature, there are a lot of algorithms: some based on a local operator analysis (Gradient, Laplacian, etc.), others on a regional analysis (histograms manipulation, regions growing, etc.), but however they have out of consideration from a contextual analysis of the whole image. It is easy to convince ourselves how such algorithms fail when the regions forming the image are more structured, for instance when those are composed of textures.

In previous papers by the authors, it has been proposed an algorithm for image segmentation based on a structural analysis. In the following we indicate with the term "structure" each region of the image that verifies one or more uniformity rules and because of this can be considered as an independent entity. It is clearly evident that the structure concept is deeply related to well known concept of "texture". From the above, a structure can be thus characterized locating a component element (piece of the structure) that repeat itself in an isomorphic way certain number of times in two dimension.

The proposed algorithm is organized in two phases:

Phase 1: In this phase all the structures presented on the image are underlined, the same for the areas not qualified as such being a transition place between one structure and another (contours of the regions).

Phase 2: In the second phase the algorithm proceeds toward a comparative analysis of the structures trying to make a corrispondenze (through similarity functions) between the individual structures found in the previous step. We will describe in this paragraph the computational aspects related to the first phase of the algorithm, underlying the fact of how is possible to optimize the performance passing from a sequential to a systolic implementation.

The algorithm starts looking for a pixel that has not yet being classified as belonging to a region. Let "p" be such a pixel, the algorithm proceeds with the formulation and verification of several hypothesis about the possibility to locate a structure starting from the neighbouring region of the pixel.

To hypothesize a structure means to try a partition (the biggest one) of the neighbouring region with elements (windows) of dimension W_r isomorphic among them.

Let A_r be the number of analogue windows, and let B_r be the total number of windows tested; the verification of the hypothesis can be obtained testing the ratio:

$$S_r = A_r / B_r$$

with a change in r , the ratio S_r will take the maximum value corresponding to the dimension W_r to which is associated the best partition approximating the region under study.

After labelling all the pixels belonging to such region with the label "k", the algorithm resume for the location of an eventual "k+1" region.

Introducing parallel processing by systolic arrays has result in a relevant contribution for the location of the partitions. In a sequential context, a partition is build from a sample piece and proceeds adding, one at the time, other isomorphic pieces. It is evident how this procedure can get higher elaboration times, in particular when the pieces defining the partition have a small dimension.

In the systolic implementation of the algorithm, it has been possible to reduce by 1/8 factor the time required for this phase. In fact, for each expansion cycle of the partition, we can verify the isomorphism between the sample piece and other pieces, potential blocks belonging to the partition. In fig. 4 is shown how the relative pixels of the 8 pieces to be compared (P_0, \dots, P_7) are each time assembled into the processor RAM. It should be noted how 128 bits of the RAM available on each processor, are subdivided in 8 different memory planes, each of which (8-bit sequential planes) can host one of the eight piece to be compared.

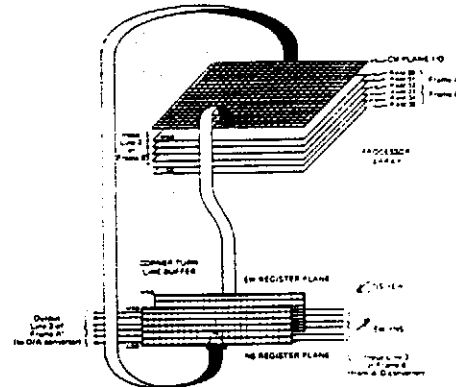


Fig. 4 Piece arrangement in the processor RAM during comparison.

CONCLUSION.

In the paper, the essential features of the systolic architecture, have been proposed, and also has been shown how this architecture can be conveniently used for digital image processing application. We must underlying on the other hand, that the state-of-art both HW and SW of this architecture has not yet reached standardized levels and put limits on more wider utilization.

According to our point of view, we will expect that in the years to come, became available systolic architectures with more advanced features, particularly with:

- 1) Higher number of integrated processors, at least 1024x1024;
- 2) Higher memory capacity for each processor;
- 3) A wider spectrum of instruction codes;
- 4) Software tools for high level programming environment on systolic processors.

REFERENCES.

- 1) M.J.B. Duff "Computing Structures for Images Processing"; Academic Press London 1983.
- 2) M.T. Kung "Why systolic architectures?"; Computer Magazine, January 1982.
- 3) S. Vitulano, A. Esposito, A. Cacace, "Structural analysis of images"; Int. Symp. on Measurement and Control, MECO-86 Taormina (Italy) 1986.
- 4) N.C.R. GAPP development System; first edition September 1985.

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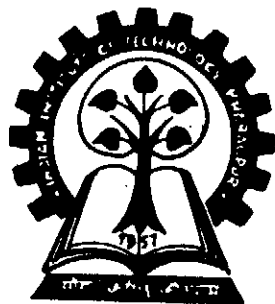
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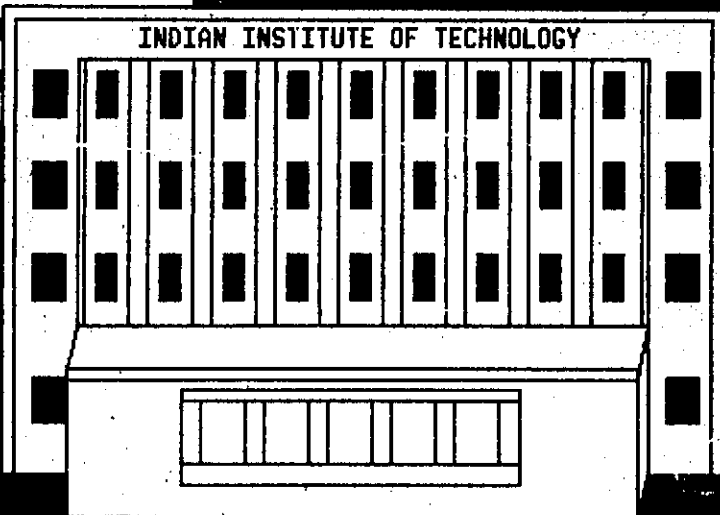
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